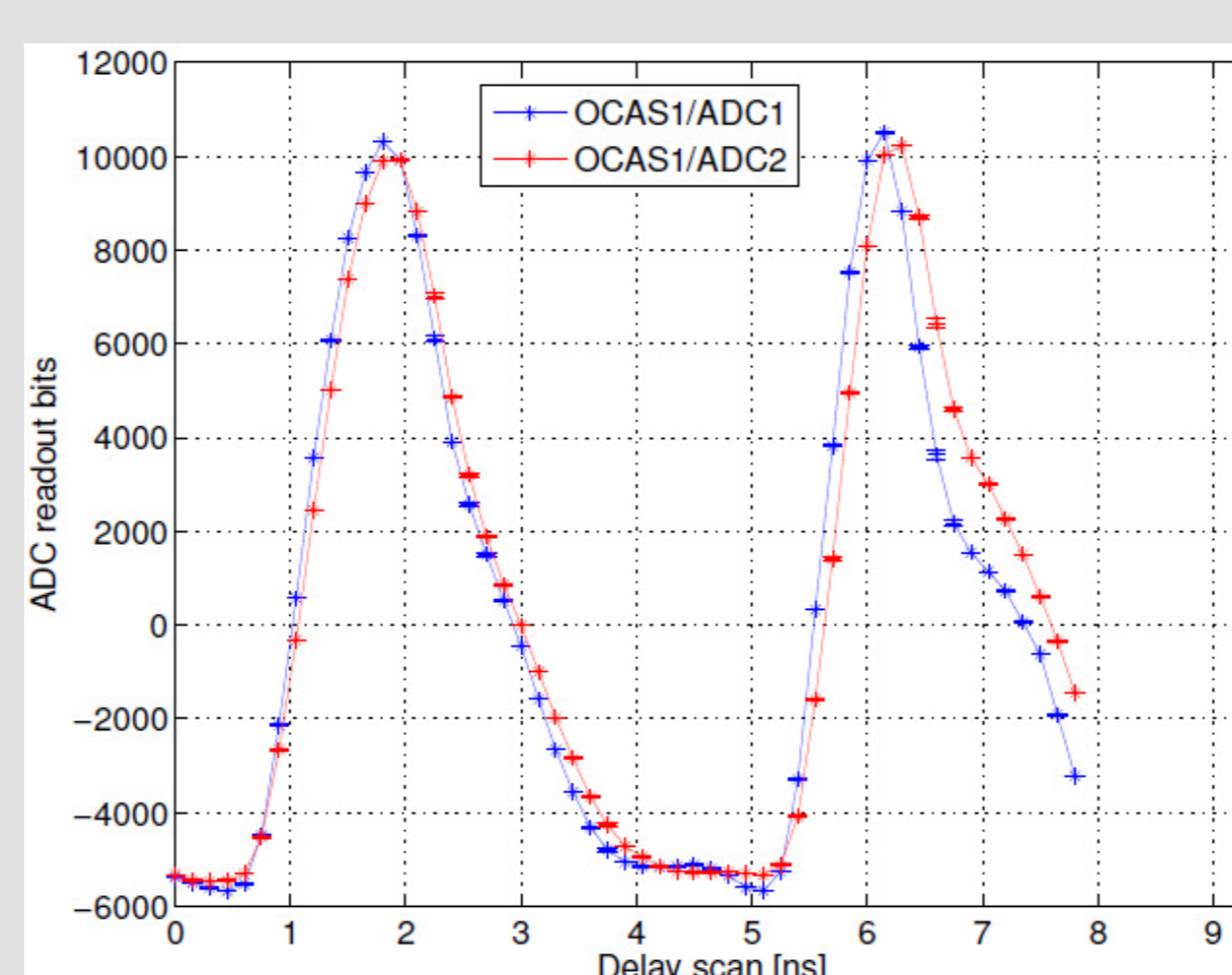


Abstract

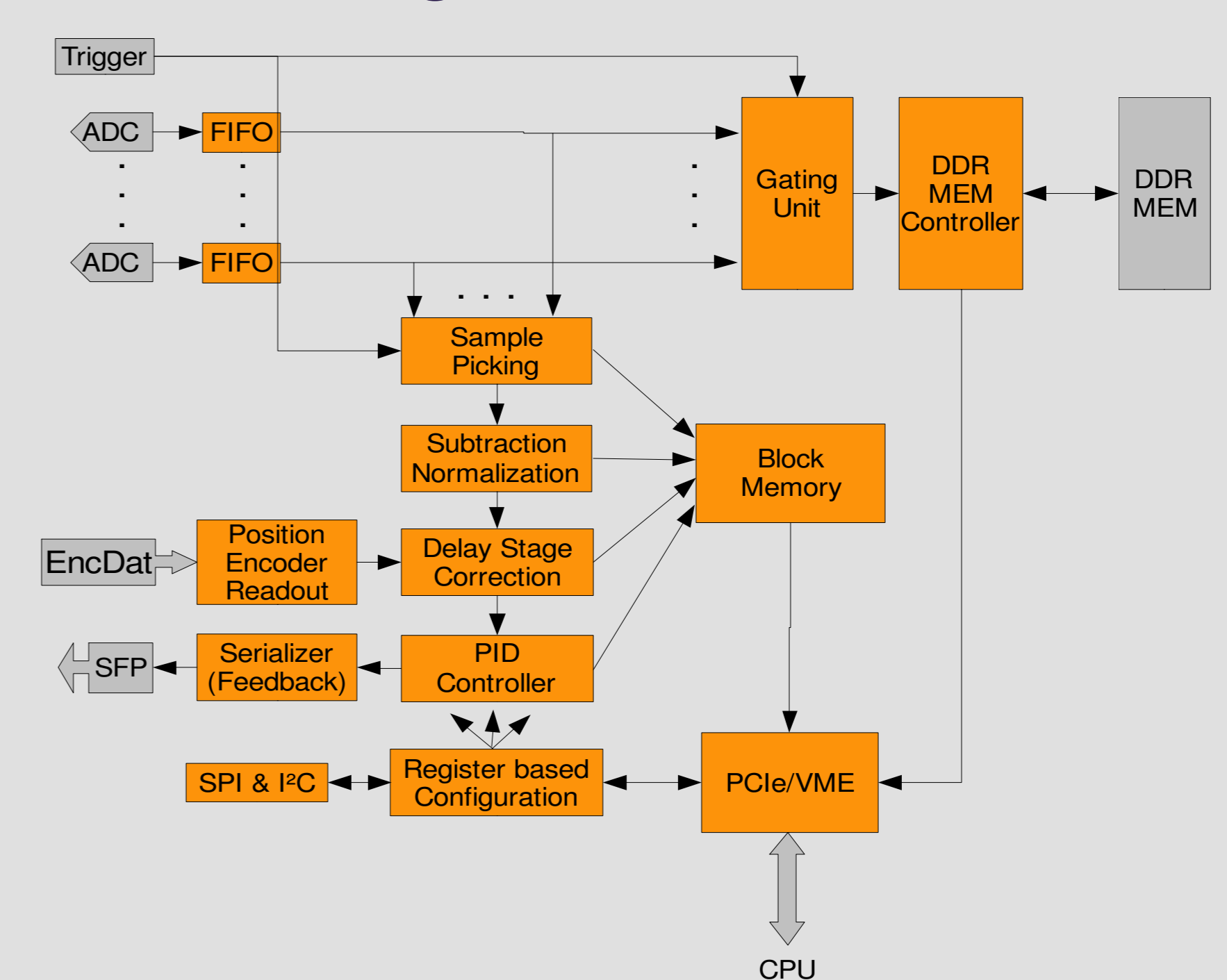
Bunch arrival-time monitors measure the arrival-time of each bunch in the electron bunch train at several locations at FLASH. The temporal reference for the monitors is provided by the optical synchronization system which distributes laser pulses with a repetition rate of 216 MHz and a length of around 200 fs FWHM. The pulses are delivered to the monitors with an arrival-time stability of about 10 fs. The bunch arrival-time is encoded as an amplitude modulation of a laser pulse from the optical synchronization system. These laser pulse amplitudes need to be sampled and processed together with additional input parameters. Because the arrival-time information is used in a feedback loop to adjust the accelerator fields, the signal processing, calibration and transmission of the bunch arrival-time information via a low-latency, high-speed link to an accelerator RF control station is needed. The most challenging problems of the signal processing are the synchronization of several clock domains, regeneration and conversion of optical laser pulses, on-line calibration, and exception handling.

Optical to Electrical Signal Conversion

- Signals from frontend are optical modulated laser pulses
- A conversion to electrical signals is performed
- Low bandwidth photodiodes do the initial conversion
- Amplification and splitting for peak and base line inputs
- Second amplification stage
- Coupling and matching of ADC input impedance



Functional Diagram



Combination of Different Clock Domains

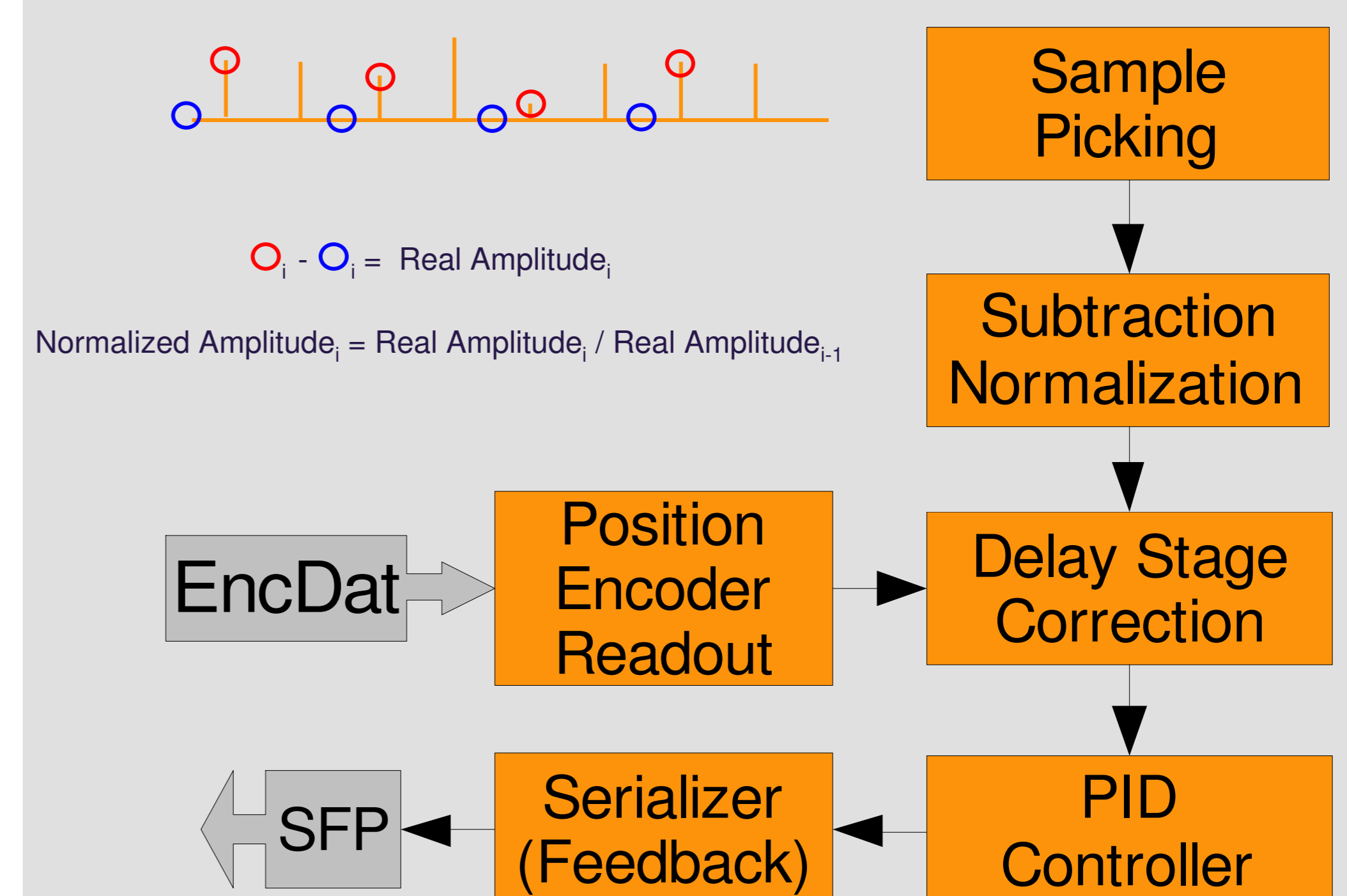
- Each ADC is running with the same frequency but with different phases
- In the FPGA all of them have to be merged into the same processing clock domain
- As the sampling is synchronized to a single trigger, no phase jumps are desired, as it results in jumps of the sample position in the data

Hardware Platforms

- Current implementation is based on digital VME carrier board (ACB2.1) with
 - Xilinx Virtex 2 Pro FPGA
 - Clock distribution with phase shifter
 - 4 ADCs with 16 Bit resolution
 - Optical to Electrical conversion
- Future implementation will be based on μ TCA platform with xTCA for Physics extensions
 - Front board:
 - 10 ADCs with 16 Bits resolution
 - Clock distribution with clock shifter
 - Xilinx Virtex 5 FPGA
 - Rear transition module with
 - Optical to Electrical conversion

Fast Feedback Processing

- In the fast Feedback, the accelerating field is influenced between bunches to stabilize the arrival time at a certain point.
- Therefore a complete processing and transmission of the arrival time information needs to be done in the FPGA



Alignment of Signals and Trigger

- Trigger is derived from Timing System and fix in time except for jitter (currently ~1ns)
- The Signals drift due to long fibers and cables
- The Signals phase is changed constantly with delay stage to adjust working point

Further Information

- Poster THPA04
- Talk THOA12
- Talk THOA3